CLAIMS

We claim:

1. A method for encoding coefficients comprising:

applying one or more wavelet transforms to generate a plurality of coefficients;

storing N bitplanes of each of the plurality of coefficients in a first memory having a plurality of rows, where each of the plurality of coefficients has a bit length greater than N bits, and wherein each storage location in each of the plurality of rows stores a bit of either a more significant bitplane of the plurality of coefficients or a less significant bitplane of the plurality of coefficients, wherein storing N bitplanes includes

storing an indication for each row of the plurality of rows to indicate a location in said each row at which bits of more significant bitplanes have started to be stored and after which bits of the plurality of coefficients of the less significant bitplanes are no longer stored.

2. The method defined in Claim 1 wherein storing of the plurality of coefficients occurs prior to identification of the number of zero bit planes in the plurality of coefficients.

3. The method defined in Claim 1 further comprising truncating bitplanes of the plurality of coefficients that are below the N bitplanes.

4. The method defined in Claim 1 wherein the indication comprises a count.

5. The method defined in Claim 4 further comprising:

counting zero bits in each of the more significant bit planes of the plurality of coefficients using a plurality of counters, wherein individual counters are associated with only one of the plurality of rows; and

stopping each counter of the plurality of counters associated with one of the most significant bitplanes when a one bit occurs in the one most significant bitplane of a coefficient.

6. The method defined in Claim 1 wherein the indication comprises a variable length code.

7. The method defined in Claim 6 wherein the variable length code indicates an amount of bits to skip until a 1-bit is encountered.

8. The method defined in Claim 6 wherein the variable length code comprises a run length code.

9. The method defined in Claim 8 wherein the run length code comprises an R2[8] code.

10. The method defined in Claim 9 wherein the first memory is 1/32 the size of a code-block.

11. The method defined in Claim 8 wherein the run length code comprises an R2[6] code.

12. The method defined in Claim 11 wherein the first memory is 1/16 the size of a code-block.

13. The method defined in Claim 1 wherein the indication for each row indicates a starting address at which bits of an associated more significant bitplane of the plurality of coefficients are stored.

14. The method defined in Claim 1 further comprising a context model accessing coefficients stored in the first memory.

15. The method defined in Claim 14 further comprising:

the context model generating an address to access a bit in the first memory; and

comparing the address with a counter value for the bitplane associated with the bit to determine if the bit is data that is not to be used by the context model.

16. The method defined in Claim 1 wherein the plurality of coefficients comprises coefficients in other than an LL subband.

17. The method defined in Claim 1 wherein the one or more wavelet transforms comprises a 5,3 transform.

18. The method defined in Claim 1 wherein the plurality of rows comprises eight rows.

19. The method defined in Claim 1 wherein the more significant bitplanes comprise bit planes 8-15 of the plurality of coefficients and the less significant bitplanes comprise bit planes 0-7 of the plurality of coefficients.

20. The method defined in Claim 1 further comprising storing the indication in the first memory.

21. The method defined in Claim 1 further comprising storing the indication in a second memory different than the first memory.

22. An apparatus for encoding coefficients comprising:

means for applying one or more wavelet transforms to generate a plurality of coefficients;

means for storing N bitplanes of each of the plurality of coefficients in a first memory having a plurality of rows, where each of the plurality of coefficients has a bit length greater than N bits, and wherein each storage location in each of the plurality of rows stores a bit of either a more significant bitplane of the plurality of coefficients or a less significant bitplane of the plurality of coefficients, wherein storing N bitplanes includes

means for storing an indication for each row of the plurality of rows to indicate a location in said each row at which bits of more significant bitplanes have started to be stored and after which bits of the plurality of coefficients of the less significant bitplanes are no longer stored.

23. The apparatus defined in Claim 22 wherein the means for storing of the plurality of coefficients stores the coefficients prior to identification of the number of zero bit planes in the plurality of coefficients.

24. The apparatus defined in Claim 22 further comprising truncating bitplanes of the plurality of coefficients that are below the N bitplanes.

25. The apparatus defined in Claim 22 wherein the indication comprises a count.

26. The apparatus defined in Claim 25 further comprising:

means for counting zero bits in each of the more significant bit planes of the plurality of coefficients using a plurality of counters, wherein individual counters are associated with only one of the plurality of rows; and

means for stopping each counter of the plurality of counters associated with one of the most significant bitplanes when a one bit occurs in the one most significant bitplane of a coefficient.

27. The apparatus defined in Claim 22 wherein the indication comprises a variable length code.

28. The apparatus defined in Claim 27 wherein the variable length code indicates an amount of bits to skip until a 22-bit is encountered.

29. The apparatus defined in Claim 27 wherein the variable length code comprises a run length code.

30. The apparatus defined in Claim 29 wherein the run length code comprises an R2[8] code.

31. The apparatus defined in Claim 30 wherein the first memory is 1/32 the size of a code-block.

32. The apparatus defined in Claim 29 wherein the run length code comprises an R2[6] code.

33. The apparatus defined in Claim 32 wherein the first memory is 1/16 the size of a code-block.

34. The apparatus defined in Claim 22 wherein the indication for each row indicates a starting address at which bits of an associated more significant bitplane of the plurality of coefficients are stored.

35. The apparatus defined in Claim 22 further comprising a context model to access coefficients stored in the first memory.

36. The apparatus defined in Claim 35 wherein the context model generates an address to access a bit in the first memory; and

further comprising means for comparing the address with a counter value for the bitplane associated with the bit to determine if the bit is data that is not to be used by the context model.

37. The apparatus defined in Claim 22 wherein the plurality of coefficients comprises coefficients in other than an LL subband.

38. The apparatus defined in Claim 22 wherein the one or more wavelet transforms comprises a 5,3 transform.

39. The apparatus defined in Claim 22 wherein the plurality of rows comprises eight rows.

40. The apparatus defined in Claim 22 wherein the more significant bitplanes comprise bit planes 8-15 of the plurality of coefficients and the less significant bitplanes comprise bit planes 0-7 of the plurality of coefficients.

41. The apparatus defined in Claim 22 further comprising means for storing the indication in the first memory.

42. The apparatus defined in Claim 22 further comprising means for storing the indication in a second memory different than the first memory.